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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,296	10/01/2002	Liang-Hua Lin	NAUP0477USA	5720

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,296	LIN ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-10* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action responds to the Amendment filed 2 February 2004.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "**20**" has been used to designate both N-type doped region and some other region in prior art Fig. 1.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: **10** in prior art Fig. 1.

3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

Paragraph [0019] is inaccurate. Lower implantation energies give smaller penetration into the substrate than higher implantation steps. Accordingly it is inaccurate to state,

> "Noticeably, the implantation energy of the first ion implantation process should be **smaller** than that of the second ion implantation process, so that the junction depth produced by the doped region 46 and the P-type epitaxial layer 34 is smaller than the junction depth produced by the doped region 42 and the P-type epitaxial layer 34."

Fig. 4 shows that the junction depth of 46 is **smaller** than that of 42 indicating that the first ion implantation energy used to form 42 is necessarily **greater** --not smaller-- than the implantation energy used to form 46.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 6, 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by US 4,415,370 (**Kagawa** et al.).

Regarding claim 1, **Kagawa** discloses a method of forming a photo sensor in a photo diode formed on a semiconductor wafer, a surface of the semiconductor comprising a substrate

with first-type dopants, and an insulating layer positioned on the surface of the substrate and surrounding the photo sensor, the method comprising:

forming a first mask layer **22** on the surface of the substrate **21** for defining positions of a plurality of first doped regions **23** in the photo sensor (Fig. 6B);

performing a first ion implantation process utilizing second-type dopants to form the plurality of first doped regions on the surface of the photo sensor (Fig. 6B);

removing the first mask layer and forming a second mask layer **22** surrounding the photo sensor (Fig. 6C); and

performing a second ion implantation process utilizing second-type dopants to form a second doped region on the surface of the photo sensor, and the second doped region being overlapped with a partial region of each of the first doped regions (Fig. 6C).

(See col. 7, line 31 to col. 8, line 11.)

Regarding claim 2, the method of claim 1 wherein the dopants in the first doped regions and in the second doped region interact with neighboring substrate to form a plurality of depletion regions (Figs. 5G, 6E).

Regarding claim 3, the method of claim 1 wherein the first-type dopants are N-type, and the second-type dopants are P-type (Figs. 6A-6F).

Regarding claim 4, the method of claim 1 wherein the first-type dopants are P-type, and the second-type dopants are N-type (Figs. 7A-7G; col. 8, lines 23-59).

Regarding claim 6, the method of claim 1 wherein a dopant density of the first ion implantation process is less than a dopant density of the second ion implantation process (Figs. 4A-4B).

Regarding claim 8, the method of claim 1 wherein the method further comprises an annealing process for driving-in the dopants in the second doped region (col. 7, lines 45-47).

Regarding claim 9, the method of claim 1 wherein each of the depletion regions formed between the neighboring first doped regions is inherently a complete depletion region, and a capacitance of each of the depletion regions is approximately equal to zero for increasing a sensing area, decreasing dark current, and further increasing photo current and photon conversion gain as admitted by Applicant in the instant specification because the **Kagawa** structure is the same structure as presently claimed. (See MPEP 2112.)

Regarding claim 10, the method of claim 1 wherein the second doped region 24 is capable of being utilized as a conducting wire of the photo sensor.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,767,538 (**Mullins** et al.) in view of **Van Zant**, Microchip Fabrication, 4th ed. McGraw-Hill: New York, 2000, pp. 72-74.

Regarding claim 1, **Mullins** discloses a method of forming a photo sensor **5** (Fig. 3A) in a photo diode **5** formed on a semiconductor wafer **50**, a surface of the semiconductor comprising a

substrate with first-type dopants, and an insulating layer positioned on the surface of the substrate and surrounding the photo sensor **5**, the method comprising:

performing a first ion implantation process utilizing second-type dopants to form the plurality of first doped regions **47** on the surface of the photo sensor **5**;

performing a second ion implantation process utilizing second-type dopants to form a second doped region **46** on the surface of the photo sensor **5**, and the second doped region being overlapped with a partial region of each of the first doped regions (Fig. 3A; col. 8, line 66 to col. 9, line 26).

Mullins does not teach that first and second masks are used to perform the first and second implantations to form the separate doped regions **46** and **47**.

Van Zant teaches that it is essential to use a patterned mask having windows formed over regions of the substrate in which ions are to be implanted while blocking the remaining regions in which no ions are to be implanted.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use first and second masks in **Mullins** to implant the separate areas **46** and **47** because the regions has different profiles and therefore require separate implantation steps, as taught by **Van Zant** to be essential.

Regarding claim 2, **Mullins** discloses the method of claim 1 wherein the dopants in the first doped regions and in the second doped region interact with neighboring substrate to form a plurality of depletion regions (Fig. 3A).

Regarding claim 3, **Mullins** discloses the method of claim 1 wherein the first-type dopants are N-type, and the second-type dopants are P-type (Fig. 3A).

Regarding claim 4, **Mullins** discloses the method of claim 1 wherein the first-type dopants are P-type, and the second-type dopants are N-type (col. 11, lines 7-10).

Regarding claim 5, **Mullins** discloses the method of claim 1 wherein the substrate further comprises an epitaxial silicon layer, and each of the first doped regions and the second doped region are formed inside the epitaxial silicon layer (col. 4, lines 30-33).

Regarding claim 8, **Mullins** discloses the method of claim 1 wherein the method further comprises an annealing process for driving-in the dopants in the second doped region.

Regarding claim 9, **Mullins** discloses the method of claim 1 wherein each of the depletion regions formed between the neighboring first doped regions is inherently a complete depletion region, and a capacitance of each of the depletion regions is approximately equal to zero for increasing a sensing area, decreasing dark current, and further increasing photo current and photon conversion gain as admitted by Applicant in the instant specification because the **Mullins** structure is the same structure as presently claimed. (See MPEP 2112.)

Regarding claim 10, the method of claim 1 wherein the second doped region is utilized to be a conducting wire of the photo sensor (Fig. 3A).

Allowable Subject Matter

9. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or suggest, in combination with the other claimed limitations, that the second implantation also forms an LDD of the logic circuit. Although it is notoriously well known to perform the implantation of an LDD simultaneously while performing the photodiode implantation, since neither Kagawa nor Mullins forms a FET, it would not be obvious to form an LDD region in either the Kagawa or Mullins photodiode systems.

Response to Arguments

11. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
22 August 2004